AMENDMENT TO THE SPECIFICATION

On page 9, please amend the paragraph commencing on line 29 as follows:

Figure 3 is a schematic block diagram of an ESD protection circuit 60 that includes an ESD disabling circuit 66, an ESD triggering circuit 64 and an ESD clamping circuit ~~66~~ 62. The ESD clamping circuit 62 is operable coupled to 1st and 2nd power pins of the integrated circuit. For instance, the 1st and 2nd power pins may correspond to the supply voltage (V_{DD}) and ground (V_{SS}). The ESD clamping circuit 62 may be a transistor, surge depressor and/or a silicon controlled rectifier. The ESD clamping circuit 62 provides a low impedance path between the 1st and 2nd power pins based on a clamping signal 68. For example, if the ESD clamping circuit 62 is a transistor, the clamping signal 68 turns on the transistor to provide a low impedance path between V_{DD} and V_{SS}. The ESD triggering circuit 64, when enabled, senses an ESD event 70 and, when such an event occurs, produces the clamping signal 68.